CLAIMS

What is claimed is:

1. A transistor comprising a gate separated from a channel by an insulator and having insulating spacers adjacent to gate sidewalls to lap portions of extension regions from a source and a drain into the channel.

2. The transistor of claim 1: (i) wherein the extension regions comprise doped extension regions; and (ii) wherein the insulating spacers comprise edges to align the doped extension regions.

3. The transistor of claim 1, wherein the insulating spacers abut the gate sidewalls.

4. The transistor of claim 1, wherein the insulating spacers have a thickness that is sufficient to reduce capacitance between the gate and the extension regions by an effective amount.

5. The transistor of claim 4, wherein the insulating spacers have a thickness that is between 10-200 Angstroms.

6. The transistor of claim 5, wherein the insulating spacers comprise an oxide of silicon.

7. The transistor of claim 6, wherein the oxide of silicon comprises silicon dioxide.

8. A transistor comprising a gate, a channel beneath the gate and separated from the gate by an insulator, a source adjacent to the channel on a first side of the gate, a drain adjacent to the channel on a second side of the gate, extension regions into the channel from the source and the drain that underlap the gate, and insulating spacers adjacent to sidewalls of the gate that overlap the extension regions.

9. The transistor of claim 8: (i) wherein the extension regions comprise doped extension regions; and (ii) wherein the insulating spacers comprise outer edges to align the doped extension regions.

10. The transistor of claim 8, wherein the extension regions comprise doped extension regions formed by doping regions of a substrate that are aligned with outer edges of the insulating spacers.

11. The transistor of claim 8, wherein the insulating spacers abut the sidewalls of the gate.

12. The transistor of claim 8: (i) wherein the insulating spacers have a thickness that is between 10-200 Angstroms; and (ii) wherein the insulating spacers comprise an oxide of silicon.

13. A transistor comprising a gate, a channel beneath the gate and separated from the gate by an insulator, a source adjacent to the channel on a first side of the gate, a drain adjacent to the channel on a second side of the gate, extension regions into the channel from the source and the drain that underlap the gate, and spacer means adjacent to sidewalls of the gate for reducing an overlap of the gate with the extension regions.

14. The transistor of claim 13 in an integrated circuit containing a second transistor that is electrically coupled with the transistor.

15. The transistor of claim 13 in a microprocessor containing a second transistor that is electrically coupled with the transistor.

16. An integrated circuit comprising:

a first transistor containing a gate separated from a channel by an insulator and having insulating spacers adjacent to gate sidewalls to lap portions of extension regions from a source and a drain into the channel; and

a second transistor electrically coupled with the first transistor.

17. The integrated circuit of claim 16: (i) wherein the extension regions comprise doped extension regions; and (ii) wherein the insulating spacers comprise outer edges to align the doped extension regions.

18. The integrated circuit of claim 17: (i) wherein the insulating spacers abut the gate sidewalls; and (ii) wherein the insulating spacers have a thickness that is between 10-200 Angstroms.

19. The integrated circuit of claim 18, wherein the insulating spacers comprise an oxide of silicon.

20. The integrated circuit of claim 19, wherein the integrated circuit comprises a microprocessor.

21. A method for fabricating a transistor comprising:

forming an insulated gate;

forming insulating spacers adjacent to sidewalls of the gate;

forming extension regions after forming the insulating spacers; and

forming a source and a drain.

22. A transistor fabricated by the method of claim 21.

23. The method of claim 21, wherein forming the extension regions after forming the insulating spacers comprises doping regions of a substrate that are aligned with outer edges of the previously formed insulating spacers.

24. The method of claim 21, wherein forming the insulating spacers comprises:

depositing an insulating layer over at least a portion of a substrate containing the insulated gate, over a top of the insulated gate, and over sidewalls of the insulated gate; and

removing the deposited layer from over the substrate and from over the top of the insulated gate while leaving the layer over the sidewalls of the insulated gate.

25. The method of claim 24: (i) wherein depositing includes depositing an oxide of silicon on the sidewalls of the insulated gate by a chemical vapor deposition; and (ii) wherein removing includes removing the portions of the oxide of silicon by an anisotropic etch.

26. A transistor fabricated by the method of claim 25.

27. The method of claim 21, wherein forming the insulating spacers comprises:

growing an insulating layer over at least a portion of a substrate containing the insulated gate, over a top of the insulated gate, and over sidewalls of the insulated gate; and

removing the deposited layer from over the substrate and from over the top of the insulated gate while leaving the layer over the sidewalls of the insulated gate.

28. The method of claim 27: (i) wherein growing includes growing an oxide of silicon on the sidewalls of the gate by thermal oxidation of silicon of the sidewalls of the insulated gate; and (ii) wherein removing includes removing the portions of the oxide of silicon by an anisotropic etch.

29. The method of claim 21, wherein forming extension regions after forming the insulating spacers comprises forming doped extension regions by using the previously formed insulating spacers as alignment masks.

30. A transistor comprising a gate, a channel beneath the gate and separated from the gate by an insulator, a source adjacent to the channel on a first side of the gate, a drain adjacent to the channel on a second side of the gate, and extension regions into the channel from the source and the drain that underlap the gate, wherein the extension regions comprise doped regions containing ions introduced into the regions into alignment with outer edges of insulating sidewall spacers adjacent to sidewalls of the gate.

31. The transistor of claim 30, wherein the insulating sidewall spacers have been removed.

32. The transistor of claim 31, wherein the insulating sidewall spacers, prior to removal, comprised an oxide of silicon and had a thickness in the range of 10-200 Angstroms.